film having a thickness not allowing carriers to transmit therethrough by the direct tunneling phenomenon;

a first control gate electrode disposed on said gate insulating film over the side wall of said floating gate electrode and over a partial surface area of said semiconductor substrate on both sides of said floating gate electrode; and

B1

a pair of impurity doped regions formed in a surface layer of said semiconductor substrate on both sides of a gate structure including said floating gate electrode and said first control gate electrode.

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3. (Amended) A semiconductor memory according to claim 1, further comprising:

a dielectric film formed on an upper surface of said floating gate electrode, said dielectric film having a thickness not allowing carriers to transmit therethrough by the direct tunneling phenomenon; and

B2

a second control gate electrode formed on said dielectric film and electrically connected to said first control gate electrode, said second control gate electrode and said floating gate electrode constituting a capacitor,

wherein said first control gate electrode is formed on said gate insulating film also over a side wall of said second control gate electrode.

B3

12. (Amended) A semiconductor memory comprising:

a semiconductor substrate;

a tunneling insulating film formed on a partial surface area of said semiconductor substrate, said tunneling insulating film having a thinness of at most 3nm;

a floating gate electrode formed on said tunneling insulating film;

a gate insulating film covering a side wall of said floating gate electrode and a partial surface area of said semiconductor substrate on both sides of said floating gate electrode, said gate insulating film having a thickness not allowing carriers to transmit therethrough by a direct tunneling phenomenon;

B3

a first control gate electrode disposed on said gate insulating film over the side wall of said floating gate electrode and over a partial surface area of said semiconductor substrate on both sides of said floating gate electrode; and

a pair of impurity doped regions formed in a surface layer of said semiconductor substrate on both sides of a gate structure including said floating gate electrode and said first control gate electrode.

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14. (Amended) A semiconductor memory comprising:

B4

a semiconductor substrate;

a tunneling insulating film formed on a partial surface area of said semiconductor substrate, said tunneling insulating film having a thinness enough to transmit carriers therethrough by a direct tunneling phenomenon;

a floating gate electrode formed on said tunneling insulating film;

a gate insulating film covering a side wall of said floating gate electrode and a partial surface area of said semiconductor substrate on both sides of said floating gate electrode, said gate insulating film having a thickness not allowing carriers to transmit therethrough by the direct tunneling phenomenon;

a first control gate electrode disposed on said gate insulating film over the side wall of said floating gate electrode and over a partial surface area of said semiconductor substrate on both sides of said floating gate electrode; and

a pair of impurity doped regions formed in a surface layer of said semiconductor substrate on both sides of a gate structure including said floating gate electrode and said first control gate electrode,

B4

wherein a surface layer of said semiconductor substrate under said first control gate electrode has a conductivity opposite to that of said impurity doped regions.